When designing such conventional CMOS logic, one of ordinary skill in the art of CMOS circuit design would not take the possible emission of light pulses from such circuits into consideration. This is because, one of ordinary skill in the art of CMOS circuit design would not be aware of the possibility of light emission from such circuits, nor the ability to use such emission to view the data being manipulated.

Thus, it is not well known to one of ordinary skill in the art of CMOS circuit design to design pMOS and nMOS transistors to be driven such that they do not have intermediate resistance simultaneously during a change of state of the CMOS structure, to manipulate the secret data, and operating conventional CMOS inverters adjacent the non-flashing CMOS structures at the same time.

Accordingly, if the Examiner is to maintain the asserted well known statement, the Examiner is again respectfully requested to provide supporting documentary evidence under MPEP §2144.03.

Regarding 35 USC 103(a) Rejections

Notwithstanding the above rebuttal of the Examiner's statement of what is purported to be well known in the art, it is further respectfully submitted that there is no motivation for one of ordinary skill in the art to modify the disclosed CMOS circuit of Park to obtain a non-flashing CMOS structure as claimed in the claimed invention.

This is because, the CMOS structure disclosed by Park, as illustrated in Fig. 3, is an example of an analogue CMOS circuit which, when turned on, will have continuous current flowing. This continuous current is necessary for the desired operation of the circuit as a word line generator. That is, there is no motivation to modify the disclosed circuit to be "non-flashing", e.g., driving the pMOS and nMOS transistors under non-synchronized clock signals as claimed in pending claims 9 and 10, as it relies on linear and continuous time amplification to provide a constant (while on) output voltage (see, for example, col. 4, line 18-col. 5, line 27 of Park).

Thus, it is respectfully submitted that the subject matter of pending claims 1-10 is not taught or suggested by Park either taken alone or in combination with what the Examiner purports as being well known.

It is respectfully submitted that all of the Examiner's rejections have been traversed. Accordingly, it is submitted that the present application is in condition for allowance and reconsideration of the present application is respectfully requested.

Very respectfully,

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source, the current being almost independent of V_{ds}. This may be verified from Eq. (2.2c) since

$$\frac{dI_{ds}}{dV_{ds}} = \frac{d\left(\frac{\beta}{2}(V_{gs} - V_t)^2\right)}{dV_{ds}} = 0. \tag{2.10}$$

The transconductance g_m expresses the relationship between output current I_{ds} and the input voltage V_{gs}, and is defined by

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}\bigg|_{V_{ds}=\text{constant}} \tag{2.11}$$

It is used to measure the gain of an MOS device. In the linear region, g_m is given by

$$g_{m\,(linear)} = \beta V_{ds}, \tag{2.12}$$

and in the saturation region by

$$g_{m\,(sat)} = \beta(V_{gs} - V_t). \tag{2.13}$$

For example, the value of transconductance for an n-type transistor in the linear region is

$$g_{m_n} = \left(\frac{\mu_n \varepsilon}{t_{ox}}\right)\left(\frac{W_n}{L_n}\right)V_{ds}. \tag{2.14}$$

Since transconductance must have a positive value, absolute values are used for voltages applied to p-type devices.

2.3 The complementary CMOS inverter — DC characteristics

A complementary CMOS inverter is realized by the series connection of a p- and n-device, as shown in Fig. 2.10. In order to derive the DC transfer characteristics for the inverter (output voltage V_O as a function of V_{in}), we start with Table 2.1, which outlines various regions of operation for the n- and p-transistors. In this table, V_{t_n} is the threshold voltage of the n-channel device, and V_{t_p} is the threshold voltage of the p-channel device. The objective is to find the variation in output voltage (V_O) for changes in the input voltage (V_{in}).

We commence with the graphical representation of the simple algebraic equations described by Eq. (2.2) for the two transistors

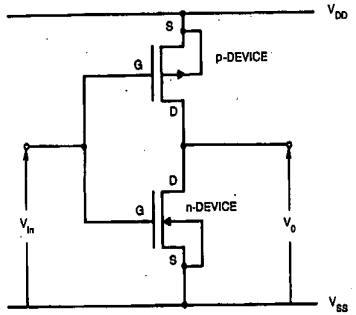

FIGURE 2.10. A CMOS inverter (with substrate connections)

shown in Fig. 2.11a [CaMi72]. The absolute value of the p-transistor drain current I_{ds} inverts this characteristic. This allows the V-I characteristics for the p-device to be reflected about the x-axis (Fig. 2.11b). This step is followed by taking the absolute value of the p-device V_{ds}, and superimposing the two characteristics yielding the resultant curves shown in Fig. 2.11c. The input/output transfer curve may now be determined by the points of common V_{gs} intersection in Fig. 2.11c. Thus, solving for $V_{in_n} = V_{in_p}$ and $I_{ds_n} = I_{ds_p}$ gives the desired transfer characteristics of a CMOS inverter as illustrated in Fig. 2.12. The switching point is typically designed to be 50 percent of the magnitude of the supply voltage: $\approx V_{DD}/2$. During transition, both transistors in the CMOS inverter are momentarily 'ON', resulting in a short pulse of current drawn from the power supply. This is shown by the dotted line in Fig. 2.12.

TABLE 2.1. Relations between voltages for the three regions of operation of a CMOS inverter

	CUTOFF	LINEAR	SATURATION
p-device	$V_{gs_p} > V_{t_p}$;	$V_{gs_p} < V_{t_p}$;	$V_{gs_p} < V_{t_p}$;
		$V_{in} < V_{t_p} + V_{DD}$	$V_{in} < V_{t_p} + V_{DD}$
	$V_{in} > V_{t_p} + V_{DD}$	$V_{gd_p} < V_{t_p}$;	$V_{gd_p} > V_{t_p}$;
		$V_{in} - V_O < V_{t_p}$	$V_{in} - V_O > V_{t_p}$
n-device	$V_{gs_n} < V_{t_n}$;	$V_{gs_n} > V_{t_n}$;	$V_{gs_n} > V_{t_n}$;
		$V_{in} > V_{t_n}$	$V_{in} > V_{t_n}$
	$V_{in} < V_{t_n}$	$V_{gd_n} > V_{t_n}$;	$V_{gd_n} < V_{t_n}$;
		$V_{in} - V_O > V_{t_n}$	$V_{in} - V_O < V_{t_n}$

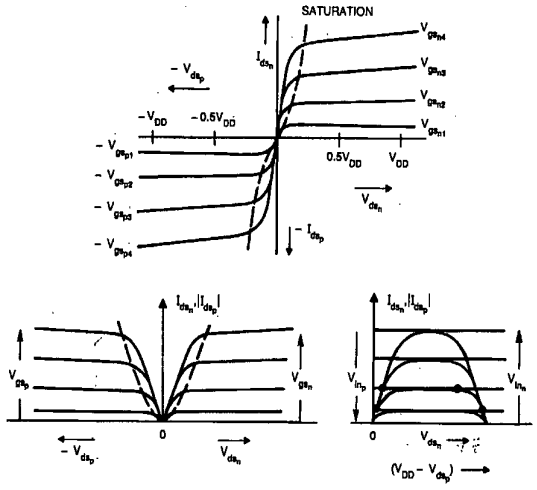

FIGURE 2.11. Graphical derivation of inverter characteristic (load line)

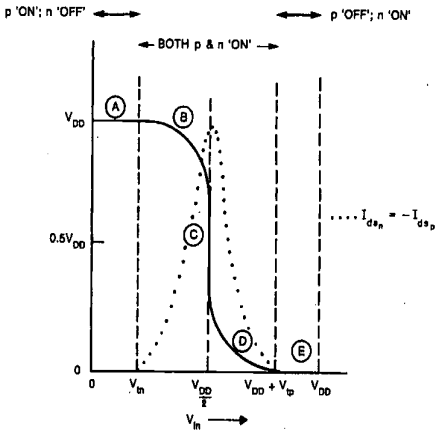

FIGURE 2.12. CMOS inverter DC transfer characteristic and operating regions

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